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Harmonic Mitigation Using a Polarized Ramp-time Current-Controlled Inverter

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Abstrak

Makalah ini menjelaskan implementasi tapis daya aktif shunt untuk sistem tiga-fasa empat-kawat untuk mengatasi masalah kualitas daya yang dihasilkan oleh beban campuran, yaitu kombinasi komponen harmonisa, daya reaktif dan tidak seimbang. Tapis ini merupakan inverter sumber tegangan terkendali arus (CC-VSI) tiga fasa dengan induktor pada keluaran AC dan kapasitor DC-bus. CC-VSI bekerja mengkontrol arus grid secara langsung agar berbentuk sinus dan sefasa dengan tegangan grid tanpa mendeteksi arus beban. Operasi saklar elektronik diatur menggunakan metode polarized ramp-time current control yang berbasis zero average current error (ZACE) dengan frekuensi penyaklaran konstan. Dari hasil percobaan laboratorium, terbukti tapis ini mampu meredam harmonisa dan daya reaktif sehingga arus grid berbentuk sinus dan sefasa dengan tegangan grid, dan seimbang walaupun tegangan grid terdistorsi.

Kata kunci*: active power filter, harmonisa, metoda current-control*

Abstract

This paper describes the implementation of a shunt active power filter for a three-phase four-wire system to overcome the power quality problems generated by mixed non-linear loads which are a combination of harmonic, reactive and unbalanced components. The filter consists of a three-phase current-controlled voltage source inverter (CC-VSI) with a filter inductor at the AC output and a DC-bus capacitor. The CC-VSI is operated to directly control the grid current in order to be sinusoidal and in phase with the grid voltage without sensing the load currents. The switching is controlled by using polarized ramp-time current control, which is based on the concept of zero average current error (ZACE) with a fixed switching frequency. The laboratory experiment results indicate that the filter is able to mitigate the harmonics and the reactive power, so that the grid currents are sinusoidal, in phase with the grid voltages, and symmetric although the grid voltage contains harmonics.

Keywords*: current-control technique, harmonics, active power filter.*

1. Introduction

Non-linear loads, especially power electronic loads, create power quality problems due to harmonic currents and voltages that deteriorate power system and its apparatus. For many years, various active power filters (APF) have been developed to suppress harmonic currents, as well as to compensate for reactive power, so that the source/grid will supply sinusoidal voltage and current with unity power factor [1], [2] ,[3].

In general, a current-controlled voltage source inverter (CC-VSI) is employed as a shunt APF to inject equal-but-opposite harmonic and reactive compensation currents based on calculated reference currents. Hence, the current sensors are installed on the load side. Then, their output signals will be processed to construct the reference or desired currents, which consist of harmonic and reactive components as well as negative- and zero-sequence components for unbalance compensation. Once the desired reference currents have been established, the currents must be injected into the grid accurately by directly controlling the inverter output current using a current control mechanism.

There are a lot of methods to generate the reference current from the load current [4]. The transformation of non-sinusoidal load currents in the *a-b-c* reference frame to the synchronously rotating *d-q* reference frame is useful in facilitating the extraction process of harmonic components from load currents [5]. Another method is the *p-q* theory introduced by Akagi [6], which is based on the instantaneous power compensation. A recent attempt has been made to apply the neural network technique [7] for separating the harmonic components from the fundamental component.

The shunt APF can also compensate for harmonic as well as reactive currents without detecting the load currents and creating harmonic-rich reference currents. The CC-VSI as a shunt APF acts to directly control the source/grid currents to be sinusoidal and in-phase with the grid voltage [8]. In this case, the current sensors are not located at the load side (for creating the harmonic reference current) but at the grid side (for controlling the grid current). Controlling the grid current rather than the inverter current allows us to create easily a sinusoidal reference current (for the grid current), rather than having to create a harmonic- and transient-rich reference current (for the inverter current). The idea to obtain the desired grid current waveform instantaneously without calculation is easily fulfilled by using an active power balanced technique. The active power is maintained balanced among the grid, the load and the DC bus of the power inverter by regulating the DC-bus voltage.

The development of a current control mechanism is important for injecting harmonic and reactive compensation current. The polarized ramp-time current control (PRCC) technique based on ZACE (zero average current error) has been established as described in the literature [9], [10], [11]. Regarding to the operation and performance of a shunt APF, the PRCC has been chosen due to its capability of minimizing ripple current using a fixed switching frequency technique so that it does not generate additional low order harmonics that deteriorate the performance of the filter. Furthermore, it has a high bandwidth and a fast transient response. Therefore, the idea of applying the PRCC to a shunt APF by directly controlling the grid current will be examined.

2. Research Method

2.1. Shunt Active Power Filter Configuration

The three-phase shunt active power filter is a three-phase current-controlled voltage-source inverter (CC-VSI) with a mid-point earthed split capacitor (C_1 and C_2) on the DC bus and inductors (L=L_{inv}) on the AC output (Figure 1). Thus, it is essentially three independent single-phase inverters with a common DC bus.

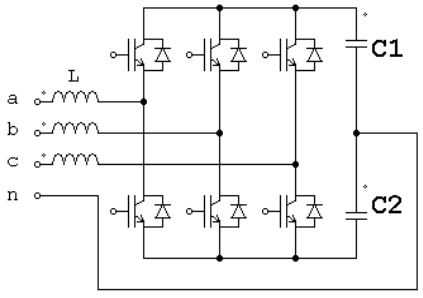

Figure 1. Three-phase Voltage Source Inverter (VSI)

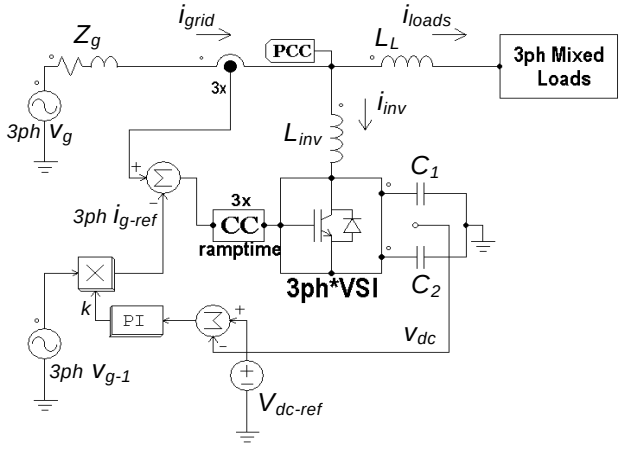

Figure 2. The shunt APF configuration

The APF consists of two control loops, namely a current control loop and a voltage control loop. The current control loop employs PRCC to shape the grid currents to be sinusoidal by generating a certain pattern of PWM for continuous switching of the inverter switches. The

upper and lower switches are operated on a complementary basis and generate PWM bi-polar voltage switching. The voltage control loop uses a simple Proportional Integral (PI) controller to keep the DC-bus voltage constant at a certain DC voltage reference and to provide the magnitude of reference current signals as well as to control the power flow. The speed of response of the voltage control loop is much slower than that of the current control loop. Hence, the current and voltage control loops are decoupled. Figure 2 shows the shunt active power filter configuration [8].

2.2. Direct Control of the Grid Current

As shown from Figure 2, the CC-VSI is connected in parallel with the grid, close to the non-linear loads. A node, which is a point of common coupling (PCC), is created with three connections, one each to the load, the grid and the converter, so that all three currents (for three or four wires) are potentially available to be directly controlled by the power converter. Hence, it would seem reasonable to control the grid current directly.

Moreover, the controllability of the grid current can be achieved using bipolar PWM switching. The upper and lower switches of each half-bridge are switched on a complementary basis. As a result, the output current of the inverter through the inductor, as well as the grid current, can always be controlled to ramp up and down continuously. Therefore, the direct control of the grid current is feasible because the switching action will have a direct, immediate and predictable effect on the grid current, and hence provide the controllability.

Thus, by putting the one current sensor per phase on the grid side, the grid currents are sensed and directly controlled to follow symmetrical sinusoidal reference signals and in-phase with the grid voltages. The grid currents are forced to behave as a sinusoidal current source and the grid appears as a high-impedance circuit for harmonics. The three-phase shunt APF can also provide complete compensation for many loads at the PCC instead of compensating for each load individually.

The system may contain significant amounts of load unbalance with non-linear single-phase loads. Such loads produce large negative- and zero-sequence currents. The shunt APF has also the ability to balance the asymmetrical current without measuring and determining the negative- and zero-sequence component. This is because the current control loop can force the grid currents to follow a three-phase balanced sinusoidal reference signal so that the inverter creates the inverse of the negative- and zero-sequence current automatically.

Hence, by forcing the grid current to be sinusoidal, the CC-VSI automatically provides the harmonic, reactive, negative- and zero-sequence currents for the load, following the basic current summation rule:

$$i_{grid}=i_{inverter} + i_{loads} \quad (1)$$

To obtain the desired grid current waveform instantaneously without significant calculation is easily fulfilled by adopting an active power balance technique among the grid, the load and the DC bus of the CC-VSI.

As shown in Figure 2, the sinusoidal grid current reference signal is given by:

$$i_{g\text{-}ref}=k\, v_{g\text{-}1} \quad (2)$$

where $v_{g\text{-}1}$ is the fundamental component of the grid voltage, and obtained from a phase-lock-loop (PLL) circuit detecting the grid voltage. The value of k is the output of a simple Proportional Integral (PI) controller, which is employed in the voltage control loop.

When an active power fluctuation drawn by the load occurs, the active power between the load and the grid will be unbalanced. The DC-bus of the CC-VSI immediately supplies (absorbs) the active power mismatch between the grid and the load, since the voltage control loop is set with a slower response and does not respond instantaneously to provide the appropriate grid reference current magnitude. This yields a DC-bus voltage deviation (ΔV_{dc}). Due to active power balance, the amplitude of grid active currents must be adjusted appropriately to compensate for the active power charged/discharged from the DC capacitors of

the inverter. The required change in grid currents will come as soon as the voltage control loop responds to change in the magnitude of the grid currents. Hence, any mismatch between the required load active current and that being forced by the CC-VSI would result in the necessary corrections to regulate the DC-bus voltage. The output of the PI controller, which is a gain *k*, can determine the amount of ΔV_{dc} that corresponds to the grid current amplitude. Finally, the active power supplied from the grid is matched to that consumed by the load. A new steady state has been achieved with a new grid current amplitude. The average DC-bus voltage is then recovered and stays at the reference voltage.

2.3. Polarized Ramp-time Current Control System

2.3.1. Operating Condition of the Current Control Loop

Neglecting the losses in the VSI, the output current for each phase (each half-bridge) of the inverter through the inductance L_{inv} can be expressed in a switching function (*s*) as:

$$\frac{di_{inv}}{dt} = \frac{1}{L_{inv}}(v_{pcc} - s\,v_{C1} - (s-1)\,v_{C2}) \tag{3}$$

s=1 if the upper switch is closed, and *s*=0 if the upper switch is open. It must be assumed that the voltage at the PCC (v_{pcc}), and the DC-capacitor voltages (v_{C1} and v_{C2}) are constant over the switching period. Values of v_{C1} and v_{C2} are always positive.

For the inverter output current to ramp up ($\frac{di_{inv}}{dt} > 0$) and ramp down ($\frac{di_{inv}}{dt} < 0$), the inverter always generates currents as long as the magnitude of both DC-capacitor voltages (v_{C1} and v_{C2}) is greater than the peak value of the PCC voltage ($v_{pcc\text{-}peak}$). If this condition is not achieved, then the required operating condition for the system is not provided, and the compensation fails completely.

2.3.2. The PRCC Description

The PRCC has characteristics similar to a sliding mode control [12]. The operation principle of PRCC is based on the concept of zero average current error (ZACE) for each switching period. A detailed description and analysis of PRCC has been explained in [9]. For application to the shunt APF, the current error signal (ε), which is the difference between the actual grid current (i_{grid}) and the sinusoidal grid reference current ($i_{g\text{-}ref}$) waveform, can be defined as a sliding surface.

$$\varepsilon = i_{grid} - i_{g\text{-}ref} \tag{4}$$

To ensure that the system can remain on the sliding surface and maintain perfect tracking, the following condition must be satisfied:

$$\varepsilon\,\dot{\varepsilon} \le 0 \tag{5}$$

where $\dot{\varepsilon}$ is derived from equation (4):

$$\frac{d\varepsilon}{dt} = \frac{di_{grid}}{dt} - \frac{di_{g-ref}}{dt} \tag{6}$$

According to equation (5), the following relationship must be true:

$$\left|\frac{di_{grid}}{dt}\right| > \left|\frac{di_{g-ref}}{dt}\right| \tag{7}$$

From the switching operation implementation, the $\dot{\varepsilon}$ is able to be controlled such that a positive value of the error signal ($\varepsilon > 0$) produces a negative derivative of the error signal $(\dot{\varepsilon} < 0)$, and a negative value of the error signal ($\varepsilon < 0$) produces a positive derivative of the error signal $(\dot{\varepsilon} > 0)$. Controlling the sign of $\dot{\varepsilon}$ is associated with controlling the sign of $\frac{di_{grid}}{dt}$ to be positive or negative. Then, combining equations (1) and (6), $d\varepsilon/dt$ can be expressed as:

$$\frac{d\varepsilon}{dt} = \frac{di_{load}}{dt} + \frac{di_{inv}}{dt} - \frac{di_{g-ref}}{dt} \tag{8}$$

Referring to the active filter operation by controlling the grid currents, the CC-VSI automatically generates output currents i_{inv} in compensating for unwanted currents in the loads. If the sign of $\frac{di_{inv}}{dt}$ and $\frac{di_{grid}}{dt}$ are matching, then perfect tracking can be achieved as long as the magnitude of the $\frac{di_{inv}}{dt}$ is greater than $\frac{di_{load}}{dt}$. This means that zero crossing of the current error signal will occur at the end of a half-switching period. Otherwise, the system is moving away from the sliding surface, and the CC-VSI loses its controllability.

PRCC can be briefly explained by referring to the current error signal (ε) in Figure 3. The error signal ramps up and down according to equation (5). Assuming fixed capacitor-voltages and inductance, with negligible variance in the reference current within one switching period, the current error signal has two distinct, constant slopes over the switching period.

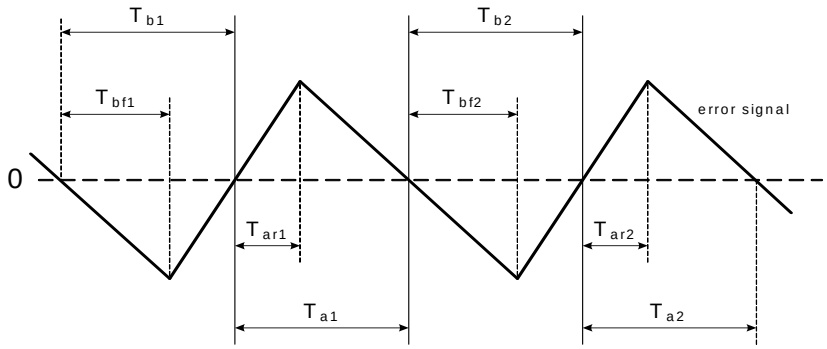

Figure 3. Current error signal

If T_a, the time the current error signal spends on one side of zero, can be made equal to T_b, the time the current error signal spends on the other side of zero, then the area of the current error signal above zero will equal the area of the current error signal below zero, and the average value of the current error signal over that switching period (T_{sw}) will be zero. Furthermore, if each of T_a and T_b can be made equal to half of T_{sw}, then switching will occur after a constant switching period and hence at a constant switching frequency. Therefore, the current error signal spends half the time on alternate sides of zero, resulting in an average value of zero, a close following of the reference signal, and a switching period (and hence switching frequency) very close to the desired value.

2.3.3. PWM Generation

In PRCC, all switching instants are timed from the information of the recently previously same-side excursion of the current error signal. Referring to Figure 3, the intended T_{bf2}, which is $T_{bf2}^{\#}$ is determined in (9) using the desired switching period T_{sw}^{*}, and the immediately previously measured values of T_{bf1} and T_{b1}, which are $\hat{T}_{bf1}$ and $\hat{T}_{b1}$. Similarly, the intended T_{ar2}, which is

$T_{ar2}^{\#}$ is determined in equation (10) using T_{sw}^{*}, and the immediately previously measured values of T_{ar1} and T_{a1}, which are $T_{ar1}^{\wedge}$ and $T_{a1}^{\wedge}$. In other words, the measured time ratio of ramps in one switching period is used to determine the next switching instant in the immediately subsequent switching period.

$$T_{bf2}^{\#} = \left(\frac{T_{bf1}^{\wedge}}{T_{b1}^{\wedge}}\right)\left(\frac{T_{sw}^{*}}{2}\right) \quad (9)$$

$$T_{ar2}^{\#} = \left(\frac{T_{ar1}^{\wedge}}{T_{a1}^{\wedge}}\right)\left(\frac{T_{sw}^{*}}{2}\right) \quad (10)$$

The performance of current control usually degrades due to switching delays. In PRCC, a switching delay in the previous switching period is inherently and automatically incorporated into the calculation of the switching instant. For instance, referring to equation (10), a switching delay causes T_{a1} to be lengthened. The result is a lower value of $T_{ar1}^{\wedge}/T_{a1}^{\wedge}$, which then produces a smaller $T_{ar2}^{\#}$ for the next switching instant, correcting for the time delay.

PRCC can be easily implemented using the ramp method of division. Equation (9) and (10) each consist of a division of two measured values, and multiplication by a constant (the switching period). Those equations are illustrated in Figure 4. If the numerator is represented by T_1, which is a fixed value, and the denominator is represented by T_2, which is a fixed ramp rate, the result is represented by the time period from when the denominator starts ramping to when the denominator equals the numerator. The ramp rate T_2 incorporates the determination of the desired switching period. From Figure 4, it is evident that T_1 is equal to the ramp rate T_2 multiplied by the time t. This then gives t as the resultant of the inputs T_1 and T_2, that is, $t=T_1/T_2$.

The functional block diagram of PRCC is described in Figure 5. The input is e_S (a binary signal indicating the polarity of the current error signal) and the output is s (a binary signal used as a command for power circuit switches).

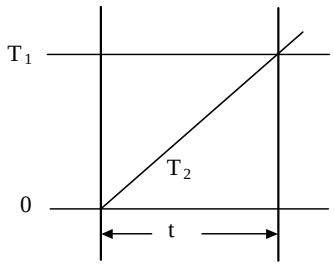

Figure 4. Ramp calculation

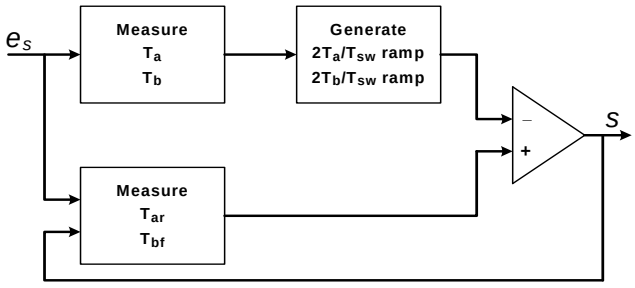

Figure 5. The functional block diagram of PRCC

3. Results and Discussion

3.1. The PRCC Operation

The simulation results of PRCC operation for the load-current sensorless active power filter are shown in Figure 6, while Figure 7 shows the experimental results. From Figure 6, it can be shown that the binary signal of e_S changes its value (1 or 0) at the zero crossing of the error signal. The time duration of the signal e_S=1 (or 0) is equal to T_a (or T_b). T_a and T_b are represented by a ramping signal with a ramp rate proportional to T_a or $T_{b,}$ respectively. T_{ar} and T_{bf} are represented by a square-wave signal, each with a magnitude proportional to T_{ar} or $T_{bf,}$ respectively. The T_{ar} signal is shown as a positive signal and the T_{bf} signal as a negative signal. The magnitude of the T_{ar} and T_{bf} signals and the ramp rate of the T_a and T_b signals are obtained from measuring those values in the previous switching period. Figure 6 also shows that if the error signal is pulled away from zero then, within the next half switching period, the switch will change to the appropriate switch position to bring the error to zero.

When s=1, and e_S becomes high, the signal $\hat{T}_{ar}$ is compared to the signal $\hat{T}_a$. When the two cross, as explained in Figure 4, s is switched low and the error signal begins ramping down. The new time duration $\hat{T}_{ar}$ has been measured for calculation for the next switching instant. Similarly, $\hat{T}_b$ and $\hat{T}_{bf}$ are used to determine when to switch s to high and the error signal begins ramping up. The new measured value of $\hat{T}_{bf}$ is then held for calculations in the next switching period.

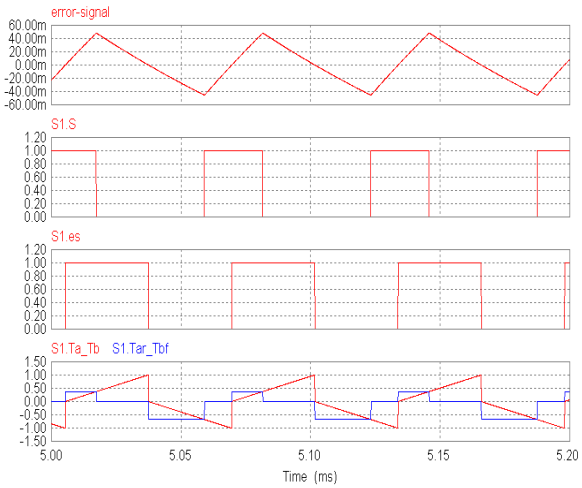

Figure 6. PRCC operation (simulation results); top to bottom: current error signal; s signal; e_S signal; signals of T_a and T_b (ramp), T_{ar} and T_{bf} (square)

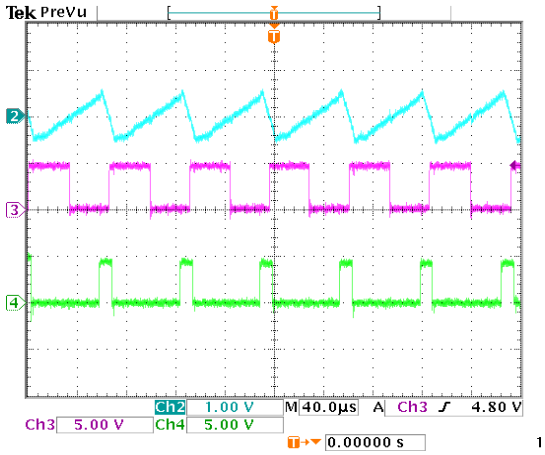

Figure 7. PRCC operation (experiment); top to bottom: current error signal; e_S signal; $\overline{S}$ signal

3.2. The Three-phase Shunt Active Power Filter Operation

The system in Figure 2 is tested using laboratory experiment to verify the shunt APF concepts. The three-phase grid voltages as shown in Figure 8 contain harmonics (THD_V=3.9%). Table 1 describes the parameter values for the system. The mixed loads contain single- and three-phase linear and non-linear loads. The linear loads are resistive and inductive loads, while the non-linear loads are a rectifier type of loads. The loads represent the distributed linear and non-linear loads, which exist in a typical electrical distribution system such as in commercial buildings. The three-phase current waveforms along with their harmonic spectrums of the mixed loads, as well as the neutral current from the laboratory experiment, are shown in Figure 9. It shows clearly that the currents are not sinusoidal. The load phase-currents are also unbalanced and contain reactive components. The significant third-harmonic current flows in the neutral wire.

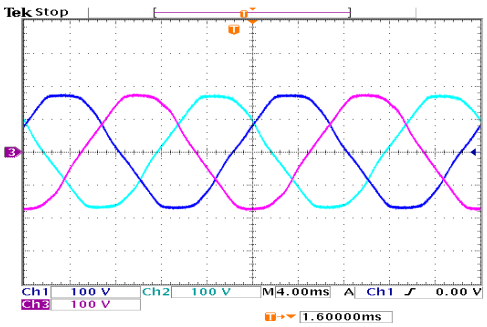

Figure 8. The grid voltages

Table 1. Parameter values for the system

Symbol	Description	Value
v_a	AC grid voltage, line-line, *rms*	207 V
f	AC line/grid frequency	50 Hz
L_L	Series inductor	0.92 mH
V_{dc}	DC-bus voltage of the inverter	480 V
C_1=C_2	DC Capacitors, electrolytic type	4000 µF
L_{inv}	Inverter inductor	1.52 mH
C_{ac}	AC filter capacitor	2 µF
f_{sw}	Target switching frequency	15.6 kHz

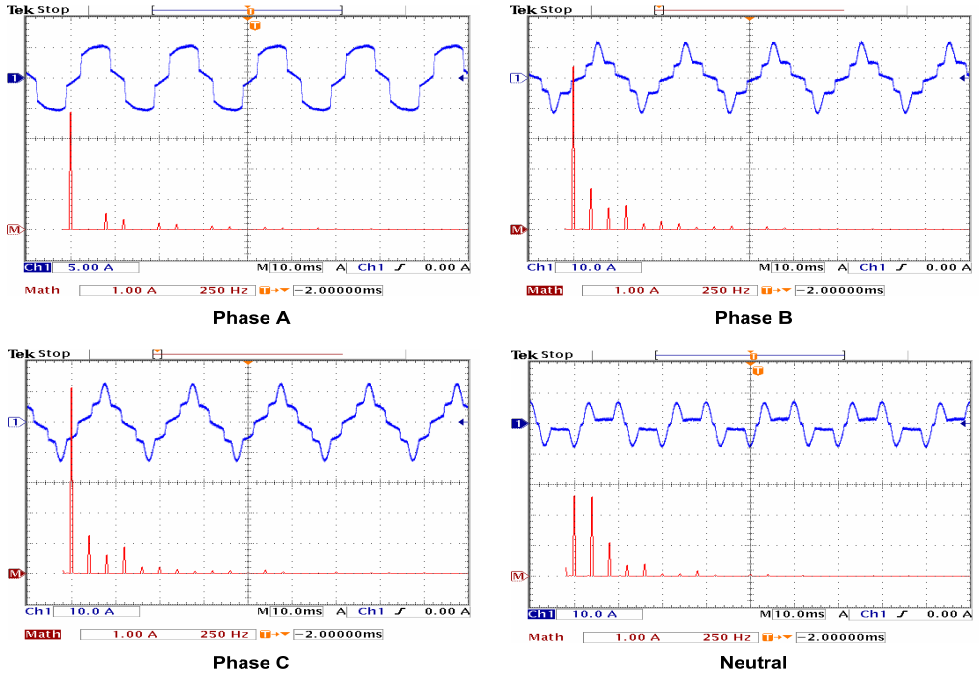

Figure 9. Phase and neutral currents for mixed loads

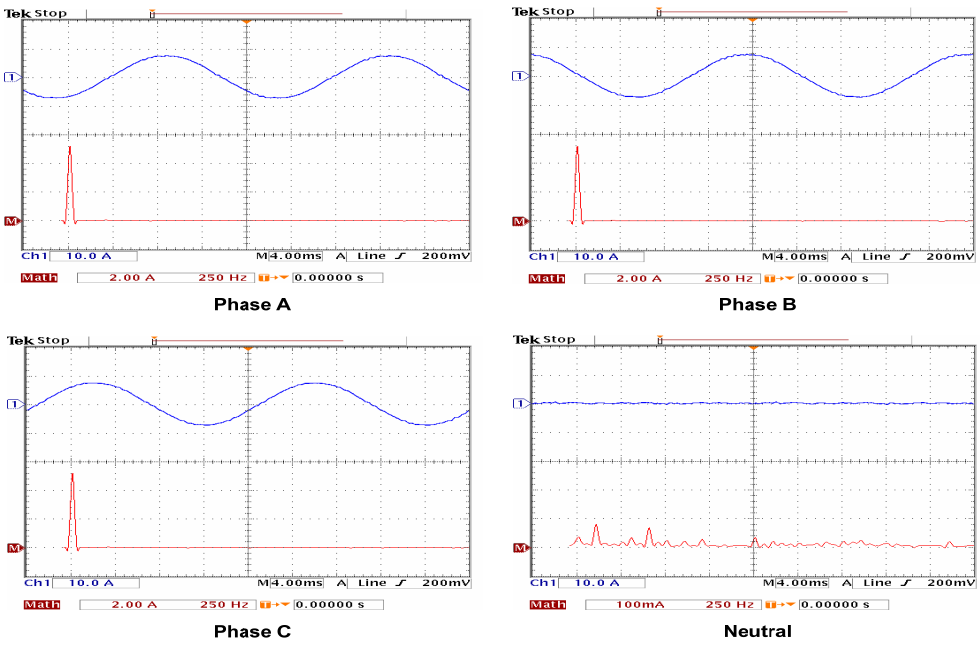

Figure 10. Phase and neutral currents of the grid after compensation

Figure 10 demonstrates the steady-state performance of compensation results. It can be shown that the shunt APF is successfully able to compensate for the harmonic, reactive and unbalanced currents produced by the total mixed loads. Although the grid voltage contains harmonics, it does not distort the grid currents. PRCC is capable to force the grid currents to follow accurately the sinusoidal reference waveforms without additional low order harmonics due to zero average current error with a fixed switching frequency. However, it produces a high frequency switching current ripple. To avoid the current ripple flowing to the grid, small AC filter capacitors (C_{ac}) are installed on the grid side. The grid currents become both sinusoidal and in

phase with the grid voltages (with insignificant phase leading by approximately 5^o due to small AC filter capacitors (C_{ac}) in Figure 11, only phase A of the grid voltage is shown).

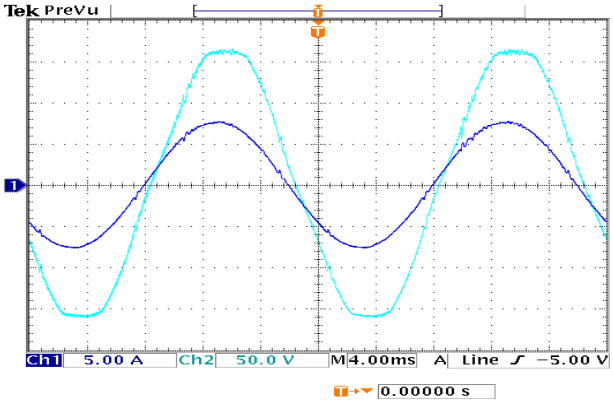

Figure 11. Phase-A grid voltage and current after compensation

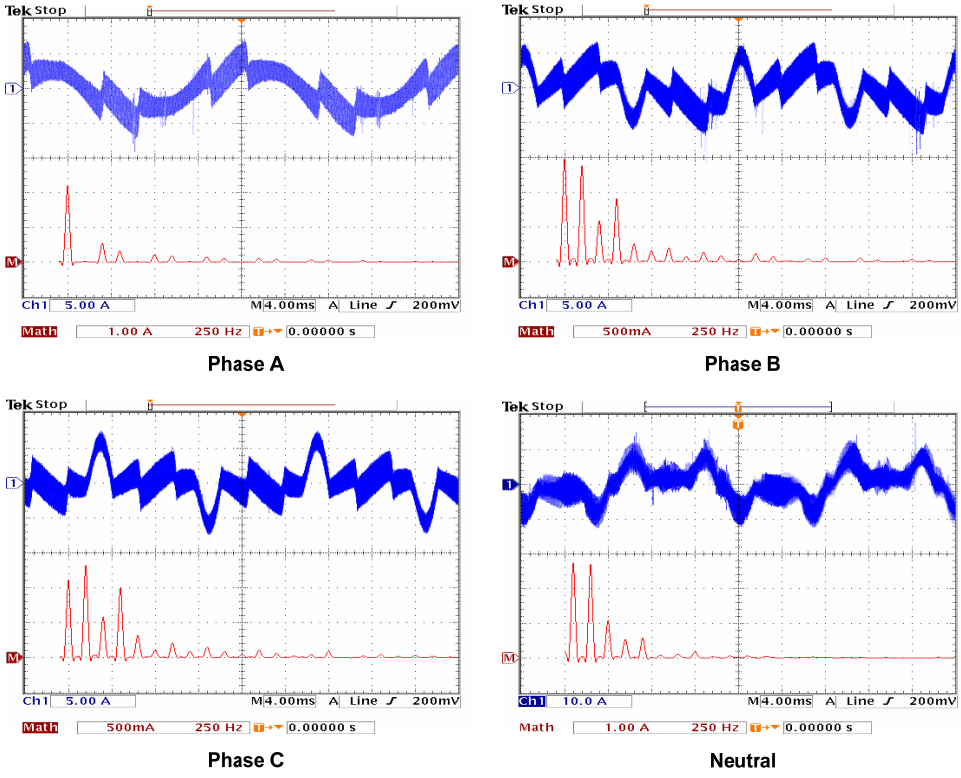

Figure 12. Phase and neutral currents of the CC-VSI

After compensation, the grid currents are symmetrical both in magnitude and phase. As a result, the neutral current at the grid is also reduced to zero. The magnitude is determined by the active power required by the system. The voltage control loop uses a simple Proportional Integral (PI) controller to keep the active power balance in the system as well as to maintain DC-bus voltage constant at a certain DC voltage reference. In this case, the values K_P and T_I of the PI controller are set to 10 and 0.007 for a stable operation. Moreover, the grid currents are balanced because the CC-VSI is operated to directly control the AC grid currents to follow a three-phase balanced sinusoidal reference signal. Once the grid currents are able to follow the

reference signals, the inverter creates the inverse of the negative- and zero sequence currents automatically to balance the unbalanced loads, without measuring and determining the negative- and zero sequence components. From Figure 12, it is obvious that the CC-VSI is able to generate three different currents for each phase as well as the neutral current. Hence, the inverter not only generates harmonics to eliminate the load harmonics but also provides balancing to create the symmetrical grid currents.

4. Conclusion

This paper explains the implementation of a three-phase four-wire shunt active power filter (APF) operated to directly control the AC grid current to be sinusoidal and in phase with the grid voltage. By doing this, the three-phase shunt APF automatically provides compensation for harmonics, reactive power and unbalance without measuring/sensing the load currents. The computational, filtering and control problems can be avoided so that the distortion and inaccuracies problems can be significantly minimized. The experimental results prove the validity of the concept.

The polarized ramp-time current control (PRCC) is very effective to shape the grid to be sinusoidal without additional low order harmonics due to the concept of zero average current error (ZACE) with fixed switching frequency. Thus, it is suitable for the grid current-controlling shunt APF.

There are many advantages to directly control the grid current. Firstly, it is easy to create a simple sinusoidal reference for the grid current using the active power balance method. The reference current is an appropriate reference to minimize the grid harmonic currents. Secondly, the grid currents produced will be sinusoidal, balanced and in phase with the grid voltage regardless of grid voltage conditions. Thus, it prevents (more) pollution of the electrical system from non-linear loads. Moreover, the control mechanism becomes very simple.

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