AUPEC 2004

Australasian Universities Power Engineering Conference
Brisbane, Australia

26-29 September 2004

ISBN 1-864-99775-3

Welcome

Welcome to the Australasian Universities Power Engineering Conference (AUPEC) 2004. The theme of this year's conference is "Challenges and Opportunities in the Deregulated Power Industry". During the last year, power industries around the world have seen a number of major blackouts. This has emphasized the importance of security in complex and interconnected power systems. New techniques and solutions are required to manage and operate the deregulated electricity industry in a market environment. This conference represents the perfect forum for presenting the strategies developed by industry and academia to meet these challenges.

Organising Committee

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A/Prof. Tapan Kumar Saha — University of Queensland

Publication Chair

Dr. Geoffrey Walker — University of Queensland

Technical Chair

Dr. Zhao Yang Dong — University of Queensland

Members

Dr. Dave Allan — Powerlink

A/Prof. David Birtwhistle	Queensland University of Technology (QUT)
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Mr. Tim George	NEMMCO
Dr. Geir Hovland	University of Queensland
Prof. Gerard Ledwich	Queensland University of Technology (QUT)
Mr. Damien Sansom	University of Queensland
Mr. Alok Thapar	University of Queensland
Mr. Zhao Xu	University of Queensland

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Foreword

MESSAGE FROM THE CHAIR - AUPEC 2004

Welcome to the Australasian Universities Power Engineering Conference (AUPEC) 2004. The theme of this year's conference is "Challenges and Opportunities in the Deregulated Power Industry". During the last year, power industries around the world have seen a number of major blackouts. This has emphasized the importance of security in complex and interconnected power systems. New techniques and solutions are required to manage and operate the deregulated electricity industry in a market environment. This conference represents the perfect forum for presenting the strategies developed by industry and academia to meet these challenges.

AUPEC is the only annual power engineering conference held in the Australasian region sponsored by the Australasian Committee for Power Engineering (ACPE). AUPEC rotates among the Universities in the Australasian region, and we are delighted to host the conference this year at the St. Lucia campus of the University of Queensland. On behalf of the organising committee, I take great pleasure in welcoming you all to Brisbane.

AUPEC provides a forum for University academics, research higher degree students and industry professionals to share innovation and developments. This year we have received over 235 digests/full papers from prospective authors from 17 countries. These countries include Australia, New Zealand, India, China, Singapore, Malaysia, Indonesia, Thailand, Iran, Germany, Austria, Italy, Turkey, Sweden, Spain, USA and Canada. Full papers were peer reviewed by national and international experts before being accepted. After a 2-stage independent peer review process, 167 papers were accepted for presentation and discussion in more than 30 technical sessions in the conference. I would like to thank all the reviewers for their time and effort in the review process, which has helped ensure an excellent technical programme across the three days of the conference.

The morning session of each day of the conference will consist of keynote sessions addressing different aspects of power system security. On the first day, the keynote session is on recent major blackouts and transmission system security. The keynote session on the second day will consider renewable energy, focusing on the challenges of wind power. The final keynote session will review the reliability issues facing the Queensland distribution system, with comments from local electricity distribution companies.

A key part of AUPEC is to provide postgraduate students with the opportunity to present their research findings. We have awarded five travel grants to students from New Zealand, Thailand, Canada, USA and Australia to help them attend the conference. This year AUPEC truly will be an international event. Prizes will also be awarded for the three best papers presented by full time students during the conference. In addition, a number of quality papers selected from this conference will be published by the Institution of Engineers Australia in a special issue of the Journal of Electrical and Electronics Engineering.

The financial support of our sponsors is gratefully appreciated. These sponsors include Energex, Duff and Macintosh Pty Ltd, NEMMCO and Ceanet. I would also like to thank the IEEE Queensland Section and the IEEE Power Engineering Society for their support. The technical co-sponsorship provided by the IEEE Power Engineering Society is highly appreciated.

I would also like to thank all the members of the AUPEC 2004 organising committee and staff members of the School of Information Technology & Electrical Engineering. Without their dedication and efforts, the conference would not have been possible.

Welcome once again. We have hope that you enjoy the Brisbane weather, which is beautiful one day and perfect the next. Finally, enjoy what we are sure will be a stimulating and worthwhile conference.

Associate Professor Tapan Saha 24 September 2004

General Chair, AUPEC 2004

Organising Committee

General Chair

A/Prof. Tapan Kumar Saha, University of Queensland

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Dr. Dave Allan, Powerlink
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Dr. Geir Hovland, University of Queensland
Prof. Gerard Ledwich, Queensland University of Technology (QUT)
Mr. Damien Sansom, University of Queensland
Mr. Alok Thapar, University of Queensland
Mr. Zhao Xu, University of Queensland

Conference Organiser

School of Information Technology and Electrical Engineering, The University of Queensland, Australia

Conference Venue

Hawken Engineering Building (Building No. 50), Staff House Road, St. Lucia Campus, University of Queensland, Brisbane, Australia

Meeting Rooms: 50-1, 50-2, 50-3, 50-N201 and 50-N202,

Registration Desk: 50-S201

Morning and afternoon teas will be served on Level 2 of the Hawken Engineering Building near the Registration Desk.

Lunches will be served at the Dinning room of St. Leo's College, located on College Road.

A notice board is situated close by the Registration Desk.

Conference Registration can be contacted on:

Phone: +61 7 3365 9217 **Fax:** +61 7 3365 4999

Email : aupec04@itee.uq.edu.au

Conference Information

AUDIO VISUAL FOR PRESENTERS

All sessions will have a PC and a digital data projector. Overhead projection equipment will also be available. All the PC's have Microsoft PowerPoint and Acrobat Reader installed; therefore, we advise you to prepare your presentation using either of these software packages.

You will NOT be permitted to connect your laptop to the data projector.

You are advised to bring your own presentation on a CD. You should load the computer with the presentation in the break before start of the session. There will be a student volunteer to help you with this.

Please hand your resume to the session chair before the start of the session, if you have not done so prior to the commencement of the conference.

Messages

All messages for delegates will be posted on a message board near the conference registration desk. Please check the board regularly. Information regarding the conference will also be displayed on the notice board.

Name Badges

Admission of delegates to all sessions, morning, afternoon teas and lunches, is by conference name badge only. Delegates are requested to wear their name badge at all times.

Opening and Keynote Speakers

Monday 27th September

Venue: 50-1

9.00 – 9.05 AM	**INTRODUCTION**	
		A/Prof. Tapan Kumar Saha
		General Chair, AUPEC 2004
9.05 – 9.15 AM	**CONFERENCE WELCOME**	
		Prof. Michael Keniger
		Executive Dean, Faculty of EPSA
9.15 – 9.30 AM	**CONFERENCE OPENING**	
		Mr Gordon Jardine
		CEO, Powerlink
9.30 – 10.30 AM	**KEYNOTE SESSION**	
		"Challenges and Opportunities in the New Transmission Business"
		Prof. George Gross
		University of Illinois, Urbana Champagne, USA

Tuesday 28th September

Venue: 50-1

9.00 – 10.30 AM	**KEY NOTE SESSION**
	"Challenges of Wind Power"
	Keynote Speaker: Mr. Jeffrey Harding
	Managing Director, Pacific Hydro
	Chair: Dr. Jennifer Crisp (NEMMCO)

VENUE: 50-1

8-30 – 9-30 AM

SPECIAL SESSION

"Australian Electric Power Institute"

Mr. Bryce Corderoy

Australian Electric Power Institute

Mr. Simon Bartlett

General Manager Network, Powerlink

Chair: Prof. Syed Islam (Curtin University of Technology)

9-30 – 10-30 AM

SPECIAL FORUM

"Reliability of Queensland Distribution System"

Emeritus Prof. Mat Darveniza

The University Of Queensland

Mr. Terry Effeney

Executive General Manager Distribution, Ergon Energy

Mr. Mike Griffin

General Manager Network Asset Management, Energex

Chair: Prof. Gerard Ledwich (QUT)

Program at a Glance

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<tr><th>Sunday 26 September</th><th>Monday 27 September</th><th>Tuesday 28 September</th><th>Wednesday 29 September</th></tr>
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<td>Workshop: "Ancillary Services in the Australian National Electricity Market"
Speaker: Bill Truscott, NEMMCO
3.00-5.00pm
Venue: 50-N201</td>
<td>Introduction: A/Prof. Tapan Saha, Conference Chair AUPEC 2004

Welcome: Prof. Michael Keniger, Exec. Dean, Faculty of EPSA

Conference Opening: Mr Gordon Jardine, CEO Powerlink

Keynote Session:
Challenges and Opportunities in the New Transmission Business
Speaker: Prof. George Gross, Univ. of Illinois, Urbana Champagne
9.00-10.30am
Venue: 50-1</td>
<td>Keynote Session:
Challenges of Wind Power
Speaker: Mr. Jeffrey Harding, MD, Pacific Hydro
Chair: Dr. Jennifer Crisp, NEMMCO
9.00-10.30am
Venue: 50-1</td>
<td>Special session: Australian Electric Power Institute
Speakers: Mr. Bryce Corderoy, AEPI
Mr. Simon Bartlett, GM Network, Powerlink
Chair: Prof. Syed Islam
Curtin University of Technology
8.30-9.30am

Special Forum: Reliability of Queensland Distribution System
Participants:
Emeritus Prof. Mat Darveniza, University of Queensland
Mr. Terry Effeney, Executive GM Distribution, Ergon Energy
Mr. Mike Griffin, GM Network Asset Management, Energex
Chair: Prof. Gerard Ledwich, QUT
9.30-10.30am
Venue: 50-1</td>
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<td>Registration
Venue: 50-S201
4.00-5.30pm</td>
<td>Morning tea
10.30-11.00am
Hawken Foyer</td>
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10.30-11.00am
Hawken Foyer</td>
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10.30-11.00am
Hawken Foyer</td>
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<td>Welcome reception
Venue:
Kathleen Rm, Staff Club, Staff House Rd, University Of Queensland, St Lucia.
6.00 pm</td>
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Monday 27 September

Lunch
Venue: St. Leo's College, College Rd
12.40-1.40pm

Paper sessions 1.40-3.20pm

PS2 50-2	PE2 50-3	PQ2 50-N201	MA1 50-N202
76	204	173	167
99	227	187	148
121	231	201	210
134	232	11	229
222	213	43	226

Afternoon Tea
3.20-3.40pm
Hawken Foyer

Paper sessions 3.40-5.20pm

CM1 50-2	PE3 50-3	MC1 50-N201	MA2 50-N202
35	224	124	48
38	165	140	54
49	175	145	181
50	230	301	70
135	182	214	

Tuesday 28 September

Lunch
Venue: St. Leo's College, College Rd
12.40-1.40pm

Paper sessions 1.40-3.20pm

PS4 50-2	RE2 50-3	MC3 50-N201	CM2 50-N202
73	194	100	161
198	200	103	178
223	218	115	179
23	233	83	235
74	20	191	142

Afternoon Tea
3.20-3.40pm
Hawken Foyer

Paper sessions 3.40-5.00pm

PQ3 50-2	PS5 50-3	MA3 50-N201
208	184	119
77	185	156
190	192	159
	141	211

Conference Dinner:
Kookaburra Queen, 7.00pm for 7.30pm

Wednesday 29 September

Lunch
Venue: St. Leo's College, College Rd
12.40-1.40pm

Paper sessions 1.40-3.00pm

MA4 50-2	SC2 50-3	PQ4 50-N201
12	217	86
26	37	96
32	53	120
72	137	146

Afternoon Tea
3.00-3.20pm
Hawken Foyer

Prize Giving AUPEC '04
Presentation AUPEC'05
Conference closing ceremony
3-20-4pm
Venue: 50-2

Social Program

REGISTRATION AND WELCOME FUNCTION

SUNDAY 26TH SEPTEMBER

4.00-5.30 PM **REGISTRATION**

VENUE: 50-S201, Hawken Engineering Building, University of Queensland

3.00 – 5.00 PM **WORKSHOP**

"Ancillary Services in the Australian National Electricity Market"

Bill Truscott

NEMMCO

VENUE: 50-N201, Hawken Engineering Building, University of Queensland

6.00 PM **WELCOME RECEPTION**

VENUE: Kathleen Room, Staff Club (Building No. 41), Staff House Rd, University of Queensland, St Lucia

Refreshments and drinks will be available.

CONFERENCE DINNER

TUESDAY 28TH SEPTEMBER, KOOKABURRA RIVER QUEEN

FROM: EAGLE ST. PIER

BOARDING: 7.00 PM

DEPARTURE: 7.30PM

RETURNING: 10.00PM

Built in the late eighties, the authentic paddle wheelers played a major role in the popular World Expo'88. The classic elegant decor and famous Queensland hospitality onboard the Kookaburra River Queens ensure a truly delightful and unique experience, which will take you back to an opulent bygone era. As evening approaches, the city lights up showing visitors the brilliance of Queensland's capital city onboard the famous River Lights Dinner Cruise.

This function has been included in the registration fee but you are kindly requested to arrange your travel to the Eagle St. Pier. Following are the options for public transport from University of Queensland to Eagle St. Pier.

How to reach Eagle St. Pier from University of Queensland:

Option 1: Catch a Bus - Route 411 (Fare A$2.40)

> **Board at:** University of Queensland. Stop 'C', Chancellors Place
>
> **Alight at:** Adelaide St., far side Creek St. (Stop 27), Walk 350 metres to Eagle St. Pier. (See map and timetable for more details)

Option 2: Catch a Ferry – City Cat (Fare A$2.40)

> **Board at:** University of Queensland Ferry Terminal
>
> **Alight at:** Riverside Ferry Terminal, Walk a few yards to the Eagle St. Pier.

Option 3: Taxi (Fare approx. A$20)

> Call a taxi (phone numbers in next section) and ask to be dropped at Eagle St. Pier in the City.

General Information

BANKING

UniCredit Union	Adjacent to Staff Club, Staff House Rd
ANZ Bank	Adjacent to Staff Club, Staff House Rd
Commonwealth Bank	Approx. 100m from Staff Club, Staff House Rd
	Additional ATM located near the Bus-Stop.

ATMs for the National Australia Bank and Westpac Bank are located near the Commonwealth Bank.

MOBILE PHONES

You are kindly requested to have your mobile phones turned off while in any of the conference sessions or workshops.

EMERGENCY MEDICAL ASSISTANCE

University of Queensland Emergency Phone Number: 3365 3333
Ambulance: 000

Health Services (St. Lucia)
8.30am-5pm, Phone: 3365 6210 (You should have a Medicare Card or Insurance to see a Doctor)

After hours private Medical Services Phone Number 3831 9999

PARKING

Parking permit must be displayed at all times while parking at the university campus. Red permit at a cost of $8 per day will be available to purchase from the Conference Office, 50-S201. You can also pay and park in different parking places within the campus. This option will be cheaper.

PHARMACY

Building No.21, Student Union Complex, Staff House Rd

POST OFFICE

Building No. 61, J. D. Story Building (near University Bus stop)

TAXIS

Yellow Cab	13 1924 (to help the driver locate the conference venue, ask the operator for "template DSTC", you will be dropped at GP South building, which is 10m from the conference venue)
Black and White Cab	131 139, 131 008
Maxi Taxi	13 6294
Silver Service	133 100

Taxi Rank is located near the University Bus-Stop.

Individual Paper Sessions

	POWER SYSTEMS (PS)
Paper ID	**Date: Monday 27 September, Time: 11.00am-12.40pm, Venue: 50-2** **PS1 Chair: Prof. Syed Islam**
150	Power System Dynamic Equivalents using Line Flow Minimization Approach *B.C. Kok, A.A. Mohd. Zin, M.W. Mustafa*
21	Incorporation of Faults in Transmission Lines with a Nonlinear Model of Power Systems *M. Aldeen, F. Crusca, R. Sharma*
24	Subsynchronous Resonance Assessment using Time Frequency Distribution Algorithm *Majid Al-Dabbagh, Nadia Yousif*
31	Load Capability and Collapse Margin Analysis of the Large Scale Queensland Power System *Craig Aumuller, Tapan Kumar Saha*
41	Comparison of Fault Location Techniques for Transmission Systems *Darren Spoor, Joe Zhu*
Paper ID	**Date: Monday 27 September, Time: 1.40-3.20pm, Venue: 50-2** **PS2 Chair: Prof. Gerard Ledwich**
76	Standard Interoperable Middleware Design for Substation Communication Systems *C.R. Ozansoy, A. Zayegh, A.Kalam*
99	A Proposal to Investigate the Problems of Three-phase Distribution Feeders Supplying Power to SWER Systems *Nasser Hossein-Zadeh, Jonathan Turner, Dawit Seyoum*
121	A New Appraoch to Stability Limit Analysis of a Shunt Active Power Filter with Mixed Non-linear Loads *Hanny H. Tumbelaka, Lawrence J. Borle, Chem V. Nayar*

134	Theoretical Investigation of Accidental Contact Between Distribution Lines of Dissimilar Voltage *V. W. Smith, V. J. Gosbell*
222	System Dynamics Modelling: Application to Electricity Transmission Network Asset Management *Jennifer Crisp, David Birtwhistle*
Paper ID	**Date: Tuesday 28 September, Time: 11.00am-12.40pm, Venue: 50-2** **PS3 Chair: A/Prof. Majid Al-Dabbagh**
75	Voltage Stability Analysis of Grid Connected Embedded Generators *Raj Kumar Jaganathan, Tapan Kumar Saha*
88	Information Embedded Power System: The Effective Communication System of the 21st Century Power System Industry *Amanullah Maung Than Oo, A. Kalam, A. Zayegh*
117	Modelling High Frequency Signal Propagation over Low Voltage Distribution Lines *R. Keyhani, D. Birtwhistle*
118	On-line Identificating of the Proportion of Dynamic Component in Composite Load Model *Shi Zhen-hui, Zhu Zhou-zhen, Zheng Jing-hong, Wang Guang, Qu Zu-yi, Wang Gang*
122	Analysis of a Series Inductance Implementation on a Three-phase Shunt Active Power Filter for Various Types of Non-Linear Loads *Hanny H. Tumbelaka, Lawrence J. Borle, Chem V. Nayar*
Paper ID	**Date: Tuesday 28 September, Time: 1.40-3.20pm, Venue: 50-2** **PS4 Chair: Prof. Victor Quintana**
73	Rapid Detection of Deteriorating Modal Damping in Power Systems *R.A. Wiltshire, P. O'Shea, G. Ledwich*
223	Modelling of the Interaction between Gas Pipelines and Power Transmission Lines in Shared Corridors *D.Markovic, V.Smith, S.Perera, S.Elphick*
23	One End Simplified Fault Location Algorithm using Instantaneous Values for Series Compensated High Voltage Transmission Lines *S. K. Kapuduwage, M. Al-Dabbagh*

198	An Open Frame Modelling Tool for Simulation of AC Power Systems *Anthony B. Morton, Robin P. Lisner, D. Grahame Holmes*
74	Monitoring of Individual Modal Damping Changes in Multi-Modal Power Systems *R.A. Wiltshire, P. O'Shea, G. Ledwich*
Paper ID	**Date: Tuesday 28 September, Time: 3.40-5.00pm, Venue: 50-3** **PS5 Chair: Dr. Craig Aumuller**
184	On-line Voltage Collapse Prediction Considering Different Kinds of Loads and On-Load Tap Changer *Momen Bahadornejad, Gerard Ledwich*
185	Identification of High Power Loads *Gerard Ledwich*
192	Iron-Cored High-Temperature Superconducting Inductors for Large Electric Power Applications *C. Chao, C. Grantham*
141	Evaluation of Economic Rent of Hydropower: A Case of Nepal *T. R. Limbu, R. M. Shrestha*
	ELECTRICITY MARKET (MA)
Paper ID	**Date: Monday 27 September, Time: 1.40-3.20pm, Venue: 50-N202** **MA1 Chair: Mr. Tim George**
167	Derivative Markets in the Australian NEM: Roles and Issues *Poh Weng Tham, Hugh Outhred, Iain MacGill*
148	Transmission Planning in Competitive Power Markets Considering the Uncertainties in Market Operation *G.B. Shrestha, P.A.J. Fonseka*
210	Using a Market Game as a Tool for Teaching Strategic Behaviour in an Electricity Industry Restructuring Course *Thai D. H. Cau, Hugh Outhred*

229	On the Development of a Web Electricity Market Simulator *M. J. Sorbello, Z.Y. Dong, X. Li*
226	Minimum Energy Quadratic Programming Method for Linear Circuits, Load Flows and Optimizing Generator Dispatch *Damien. C. Sansom, Tapan K. Saha*
Paper ID	**Date: Monday 27 September, Time: 3.40-5.20pm, Venue: 50-N202** **MA2 Chair: Mr. David Bones**
48	Markets for the Transmission Rights: Competitive Equilibrium Models *Guillermo Bautista, Victor H. Quintanay, Jose A. Aguado*
54	Loss Allocation based on Network Reduction in Deregulated Electricity Market *V. Lim, T. K. Saha, T. Downs*
181	Power System Planning and Operation in Deregulated Environment *Z. Xu, Z. Y. Dong*
70	Multiple Model Forecasting of Australian Regional Wholesale Electricity Prices *D. C. Sansom, T. K. Saha, T. Downs*
Paper ID	**Date: Tuesday 28 September, Time: 3.40-5.00pm, Venue: 50-N201** **MA3 Chair: Dr. Ian Rose**
119	Understanding Spot Price Behaviour in the Australian National Electricity Market *L. F. Sugianto, V. C. S. Lee, X. B. Lu* salah ketik, seharusnya: "L.F. Sugianto, M. Widjaja, X.B. Lu"
156	A System for Electricity Trading using Genetic Algorithm and Reinforcement Learning *A. Hryshko, T. Downs*
159	Social Analysis on Electricity Market Mechanism in Indonesia *Fidiarta Andika, Ratna Dewanda*
211	Integrated Power Scheme Simulator for Human-System Integration Studies *Rizah Memisevic, Sanjib Choudhury, Penelope Sanderson, William Wong*

Paper ID	**Date: Wednesday 29 September, Time: 1.40-3.00pm, Venue: 50-2** **MA4 Chair: Dr. Geir Hovland**
12	Flexible Interconnections for the Deregulated Electricity Market *J.Arrillaga, N.R.Watson, Y.H.Liu, B.Perera*
26	Advanced Tools to Manage Power System Stability in the National Electricity Market *Tim George, Jennifer Crisp, Gerard Ledwich*
32	Forecasting Electricity Consumption: A Comparison of Models for New Zealand *Zaid Mohamed, Pat Bodger*
72	Monte-Carlo Simulation and its Application in Modelling Electricity Market Behaviour *Ian Rose, Margarida Pimentel, David Bones*
	STABILITY AND CONTROL (SC)
Paper ID	**Date: Tuesday 28 September, Time: 11.00am-12.40pm, Venue: 50-N201** **SC1 Chair: Prof. S. P. Ghoshal**
71	A Flexible and Temporal Integral Optimal Reactive Power Control System *Mu Lin, Sandhya Samarasinghe, Ramesh K. Rayudu, Aiguo Hu*
106	The Vector Control Techniques for Low Voltage IPM Machine in 42V System *Rukmi Dutta, Faz Rahman*
113	Encoder-Less Operation of a Direct Torque Controlled IPM Motor Drive with a Novel Sliding Mode Observer *Zhuang Xu*
127	Investigation of the Behaviour of an AVR in a Ballast Load Frequency Controlled Stand Alone Micro-Hydroelectric System *Rob Jarman, Paul Bryce*
129	Effect of SMES Unit in Improving Generator Damping and Supressing SSR of HVDC Systems *A. Abu-Siada, S. Islam, W.B. Lawrance*

Paper ID	**Date: Wednesday 29 September, Time: 1.40-3.00pm, Venue: 50-3** **SC2 Chair: Dr. Jennifer Crisp**
217	Maximizing Static Voltage Stability Margin in Power Systems using a New Generation Pattern *Arthit Sode-Yome, Nadarajah Mithulananthan*
37	DSP Controlled Variable Speed Constant Frequency Induction Generator for Wave Energy Applications *S. Srinivasa Rao, B. K. Murthy*
53	A Novel Approach for Optimization of Proportional Intregral Derivative Gains in Automatic Generation Control *S.P. Ghoshal, N.K. Roy*
137	The Dynamic Stability Analysis of Induction Generators *Dawit Seyoum, Nasser Hossein-Zadeh, Peter Wolfs*
	POWER ELECTRONICS (PE)
Paper ID	**Date: Monday 27 September, Time: 11.00am-12.40pm, Venue: 50-3** **PE1 Chair: A/Prof. Fazlur Rahman**
56	Evaluation of DSP and FPGA based Digital Controllers for a Single-Phase PWM Inverter *Ariawan Tjondronugroho, Adnan Al-Anbuky, Simon Round, Richard Duke*
147	Distortion in Single Phase Hysteretic Current Control PV Inverters for Grid Connection *R. Sharma, T. Ahfock*
168	Implementation of the HEPWM Technique on a Multilevel Inverter Using FPGA *F. Salim, N.A. Azli*
176	An Investigation of Battery Voltage Equalisation Topologies for an Electric Vehicle *Ming-Kuang Hsieh, Simon Round, Richard Duke*
188	A New Efficiency Model of a Regenerative Dynamometer *Mark Croft, Geoffrey Walker, Geir Hovland*

Paper ID	**Date: Monday 27 September, Time: 1.40-3.20pm, Venue: 50-3** **PE2 Chair: A/Prof. Peter Wolfs**
204	A Low Cost Portable Car Heater based on a Novel Current-Fed Push-Pull Inverter *Aiguo Patrick Hu, Ping Si*
227	A Class E Resonant Inverter for use as Electronic Fluorescent Lamp Ballast *B.D. Singer, G.R. Walker*
231	Matrix Converter for ISA 42 V Powernet Vehicle Electrical Systems Part I: Theoretical Feasibility *Keping You, M. F. Rahman*
232	Matrix Converter for ISA 42 V Powernet Vehicle Electrical Systems Part II: Simulated Physical Implementation *Keping You, M. F. Rahman*
213	DSP-based Speed Control of a Four-Phase 8/6 Switched Reluctance Motor Drive *P. Chancharoensook, M. F. Rahman*
Paper ID	**Date: Monday 27 September, Time: 3.40-5.20pm, Venue: 50-3** **PE3 Chair: A/Prof. Richard Duke**
224	Two Stage Unity Power Factor Rectifier Design *C. D. Lister, G. R. Walker*
165	Design Considerations in an Indirectly Coupled Multilevel Motor Controller *Jordan Pierce, Geoffrey Walker, David Finn, Paul Sernia*
175	Load Dump Transient Behaviour of a 42V Prototype Integrated Starter Alternator *C. P. Mudannayake, M. F. Rahman, B. Karanayil*
230	Digital PWM Waveform Generation using Adders, Not Counters *Geoffrey Walker*
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A NEW APPROACH TO STABILITY LIMIT ANALYSIS OF A SHUNT ACTIVE POWER FILTER WITH MIXED NON-LINEAR LOADS

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Abstract

In this paper, a new approach to evaluate the operation of a shunt Active Power Filter (APF) is presented. The filter consists of a three-phase current-controlled voltage source inverter (CC-VSI) with a filter inductance at the ac output and a dc-bus capacitor. The CC-VSI is operated to directly control the ac line current to be sinusoidal and in phase with the grid voltage. The compensation is successful if the current and voltage controller operates within the stable and controllable area. The area boundaries are established from current control loop equations and voltage control loop transfer function. The simulation results indicate that the new approach is simple for analyzing the stability and controllability of the system for various loads and system parameters.

1. INTRODUCTION

Non-linear loads, especially power electronic loads, create harmonic currents and voltages in power systems. In many cases, non-linear loads consist of combinations of harmonic voltage sources and harmonic current sources, and may contain significant load unbalance (ex. single phase loads on a three phase system).

For many years, various active power filters (APF) have been developed to suppress harmonic currents, as well as compensate for reactive power, so that the source/grid will supply sinusoidal voltage and current with unity power factor [1, 2]. With mixed non-linear loads, it has been shown that a combined system of a three-phase line-current-forcing shunt APF with a series reactor installed at the Point of Common Coupling (PCC) is effective in compensating harmonic current sources, as well as harmonic voltage sources [3]. The filter is able to handle the load unbalanced as well. Figure 1 shows the filter configuration.

The filter consists of two control loops, namely an inner control loop and an outer control loop. The inner control loop is a ramptime current control that shapes the grid currents to be sinusoidal, while the outer control loop is a simple PI control to keep the dc bus voltage constant and to provide the magnitude of reference current signals.

The active power filter is able to successfully compensate the harmonics as well as the unbalance of the non-linear loads, if the two loops are controlled in a stable and controllable region. The region has boundaries/limits that are established from the inner loop equations and the outer loop transfer function. The stability and controllability of the system can be evaluated by checking whether the two loops are working within the boundaries. This new approach is simple in analysing the stability and controllability of the system for various loads and system parameters.

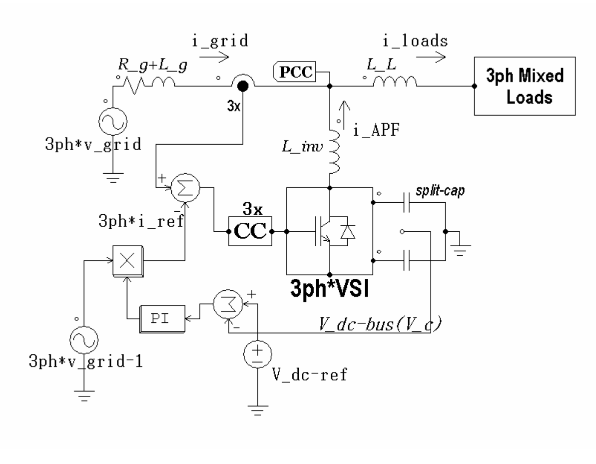

Figure 1 Active Power Filter configuration

2. A THREE-PHASE SHUNT ACTIVE POWER FILTER

The three-phase shunt active power filter is a three-phase four-wire current-controlled voltage-source inverter (CC-VSI) with a mid-point earthed, split capacitor in the dc bus and inductors in the ac output.

In Figure 1, the CC-VSI is operated to directly control the ac line/grid current to be sinusoidal and in phase with the source voltage. In this scheme, the grid current is sensed and directly controlled to follow symmetrical sinusoidal reference signals. Hence, by putting the current sensors on the grid side, the grid current is forced to behave as a sinusoidal current source and as a high-impedance circuit for the harmonics. By this principle of forcing the grid current to be sinusoidal, the APF automatically provides the harmonic, reactive, negative and zero sequence currents for the load, because

$$i_{grid} = i_{APF} + i_{loads} \tag{1}$$

The sinusoidal line current reference signal is given by:

$$i_{ref} = k\ \ v_{grid\text{-}1} \tag{2}$$

where $v_{grid\text{-}1}$ is the fundamental component of the grid voltage, and k is obtained from an outer control loop regulating the CC-VSI dc-bus voltage. This can be accomplished by a simple PI control loop. This is an effective way of determining the required magnitude of active current required, since any mismatch between the required load active current and that being forced by the CC-VSI would result in the necessary corrections to regulate the dc-bus voltage.

Another important component of this system is the small-added series inductance L_L. Without this inductance, load harmonic voltage sources would produce harmonic currents through the line impedance, which could not be compensated by a shunt APF. Currents from the APF do not significantly change the harmonic voltage at the loads. The series inductance L_L provides the required voltage decoupling between load harmonic voltage sources and the PCC. Assuming that grid voltage is balanced and sinusoidal, the equivalent circuit, from the low order harmonic point of view, is shown in Figure 2.

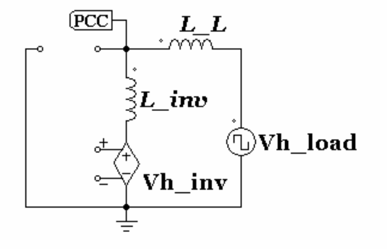

Figure 2 Equivalent circuit for low order harmonics

3. CURRENT CONTROL LOOP

The performance and effectiveness of the filter are enhanced by the use of the ramptime current control technique to control the CC-VSI [4]. The principle operation of ramptime current control is based on ZACE (zero average current error). The current error signal is the difference between the actual current and the reference signal. This error signal is forced to have an average value equal to zero with a constant switching frequency. Ramptime current control maintains the area of positive current error signal excursions equal to the area of negative current error signal excursions, resulting in the average value of the current error signal being zero over a switching period. The switching period (or frequency) is also kept constant based on the choice of switching instants relative to the zero crossing times of the current error signal.

In order to evaluate the current control to maintain the switching operation, the single-phase equivalent circuit as shown in Figure 3 is examined.

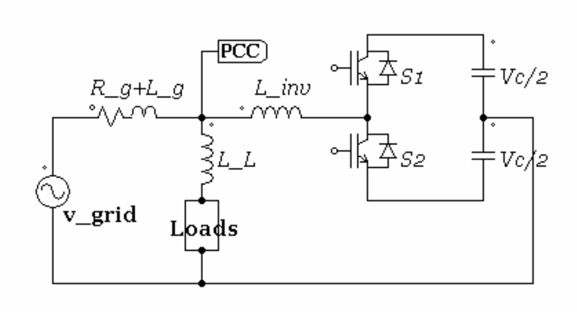

Figure 3 Current-control circuit equivalent

The output current of the inverter through L_{inv} is

$$\frac{di_{APF}}{dt} = -\frac{v_{PCC}}{L_{inv}} + (2s-1)\frac{v_C}{2L_{inv}} \tag{3}$$

where s = 1 if the upper switch is closed, and s = 0 if the upper switch is open. The switches are operated on a complementary basis. The inverter can always generate currents and the current control loop is stable as long as $v_C/2 > V_{PCC\text{-}pk}$. In this case, L_L is considered as a part of the loads.

The ramptime current control has characteristics similar to a sliding mode control. Therefore, the current error signal, ε as a controlled parameter can be defined as a sliding surface [5].

$$\varepsilon = i_{grid} - i_{ref} \tag{4}$$

To assure that the system can remain on the sliding surface and maintain perfect tracking, the following condition must be satisfied:

$$\varepsilon\,\dot{\varepsilon} \le 0 \tag{5}$$

where $\dot{\varepsilon}$ is:

$$\frac{d\varepsilon}{dt} = \frac{di_{loads}}{dt} + \frac{di_{APF}}{dt} - \frac{di_{ref}}{dt} \tag{6}$$

A positive value of the error signal (ε) produces a negative derivative of the error signal, and a negative value of ε produces a positive derivative of ε. In both cases, full controllability is achieved when:

$$\left|\frac{di_{loads}}{dt}+\frac{di_{ref}}{dt}\right|<\left|\frac{di_{APF}}{dt}\right| \qquad (7)$$

3.1 The Boundaries of Controllability

The right side of (7) represents the boundaries or limits of controllability, which are determined by the switch position s (1 or 0), v_{PCC}, v_C and L_{inv} (equation 3) and expressed in Figure 4 for $V_{PCC\text{-}rms}$ = 1pu, $V_{C\text{-}dc}$ = 3.3333 pu, X_{inv} = 1%, f = 50Hz with s = 1 (upper curve) and s = 0 (lower curve). So from (7), the current control will force the grid currents to track the reference signals perfectly, if the *di/dt* of the loads (assuming di_{ref}/dt is negligible) is between the upper and lower curves of the boundaries.

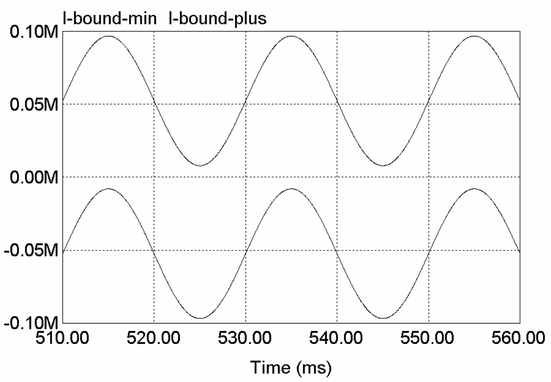

Figure 4 The boundaries of controllability

The lowest value of the upper curve has the same magnitude as the highest value of the lower curve. If this limiting magnitude is considered, the relationship between v_C and v_{PCC} for X_{inv} = 1% (0.01pu) and system frequency = 1Hz (= 1pu) to create the boundaries of *di/dt* (per-unit value – A(pu)/sec) can be depicted in Table 1 and Figure 5. The reactance X_{inv} is used rather than inductance L_{inv} because the per-unit reactance is a relative value that can be compared across different voltage and power levels or line frequencies. Therefore, the frequency is also expressed in per-unit value to provide the correct per-unit *di/dt*. For 50Hz, 60Hz or 400Hz system, the chart will be obtained by multiplying the value in table 1 with 50, 60 or 400. From the figure, it can be seen that the higher the V_C and the lower the V_{PCC}, the more margin is available for di_{load}/dt.

For X_{inv} other than 1%, the chart will be inversely proportional to the X_{inv} value. Figure 6 shows the boundaries of controllability for different values of X_{inv} (f = 1pu, $V_{PCC\text{-}rms}$ = 1pu, and $V_{C\text{-}dc}$ = 3.3333pu).

Table 1 The boundaries of controllability in A(pu)/sec with X_{inv} = 1%, f = 1Hz

Vc-pu	Vpcc-rms-pu				
	0.9	0.95	1	1.05	1.1
3.1250	182.042	137.612	93.176	48.753	4.323
3.2292	214.778	170.349	125.913	81.489	37.059
3.3333	247.390	202.960	158.530	114.100	69.670
3.4375	280.220	235.790	191.354	146.931	102.501
3.5417	312.956	268.526	224.090	179.667	135.237

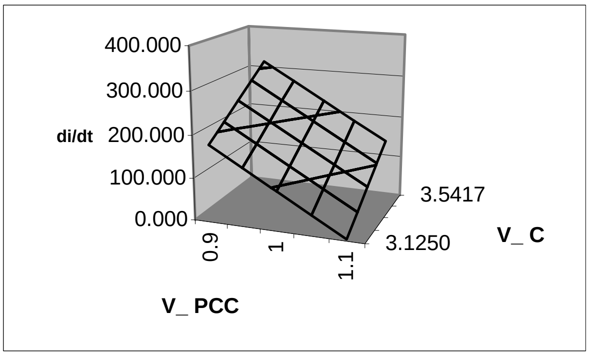

Figure 5 The boundaries of controllability in A(pu)/sec with X_{inv} = 1%, f = 1pu

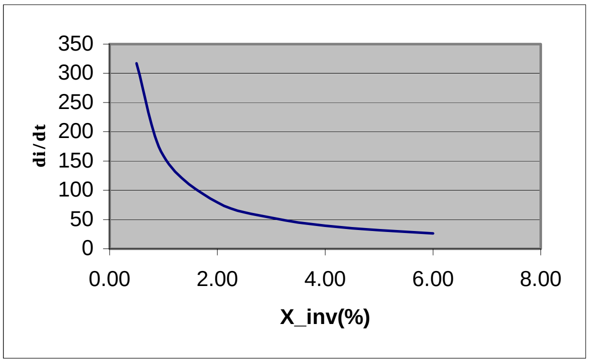

Figure 6 The boundaries of controllability in A(pu)/sec for various X_{inv}

3.2 The Effects of v_C and v_{PCC} Ripples

v_C contains low order frequency ripples. The ripples represent the active alternating power for each cycle of operation and the active power demand during transient periods. Generally, the size of the dc-bus capacitor is sufficient large to minimize the ripple. As long as $v_C/2 > V_{PCC\text{-}pk}$, the system is stable and controllability can be achieved. Hence, although v_C contains ripple, it just has to be sufficiently large so as to outweigh the fluctuation of v_{PCC} and small perturbations.

Ripples in the v_{PCC} exist due to switching actions. To analyse the high-frequency ripple in v_{PCC}, consider the portion of the circuit diagram in Figure 1 around the PCC (Figure 7):

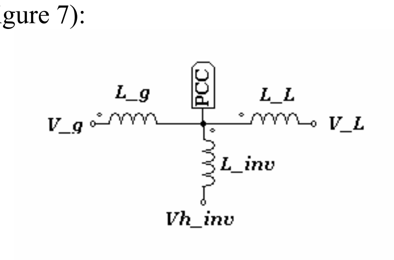

Figure 7 v_{PCC} ripple circuit

$$v_g - v_{PCC} = L_g \frac{di_g}{dt} \tag{8}$$

$$v_{PCC} - v_{h\_inv} = L_{inv} \frac{di_{APF}}{dt} \tag{9}$$

$$v_{PCC} - v_L = L_L \frac{di_L}{dt} \tag{10}$$

$$\frac{di_g}{dt} = \frac{di_{APF}}{dt} + \frac{di_L}{dt} \tag{11}$$

$$v_{PCC} = \frac{v_g + \frac{L_g}{L_{inv}} v_{h\_inv} + \frac{L_g}{L_L} v_L}{1 + \frac{L_g}{L_{inv}} + \frac{L_g}{L_L}} \tag{12}$$

$v_{h\_inv} = +v_C/2$ for $s = 1$ and $-v_C/2$ for $s = 0$

From (12), the waveform of v_{PCC} can be shown in Figure 8a. It is obvious that the ripple reduces the boundaries of controllability, because the value of v_{PCC} increases. A small high pass filter (with low losses) should be installed to eliminate the grid current ripple. By doing this, the ripple in v_{PCC} will be greatly attenuated (Figure 8b).

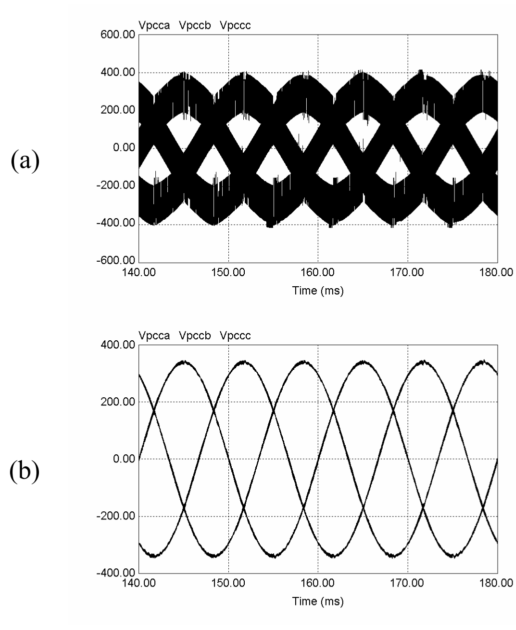

Figure 8 v_{PCC} (a) with the switching ripple; (b) the switching ripple is attenuated

4. VOLTAGE CONTROL LOOP

The outer voltage control loop employs a PI controller to adjust the gain *k* of the reference currents in order to maintain the desired dc bus voltage. The outer loop block diagram using an average model and considering a perfect tracking current control loop is shown in Figure 9. To obtain a smooth gain *k* for the dc link voltage regulator, a first order low pass filter is added to the feedback loop. The low pass filter creates a time delay T_{LPF}, which is related to the cut-off frequency of the filter.

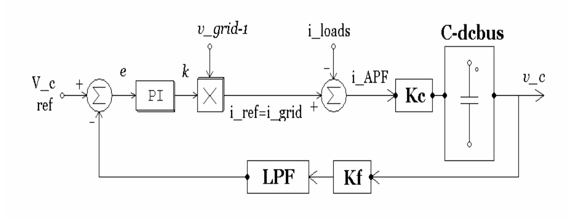

Figure 9 Outer loop block diagram

From the block diagram, the stability of the system can be evaluated through the input-output transfer function. The transfer function is observed primarily due to the dynamic changing of the loads. In this case, losses in the converter and energy stored in L_{inv} are neglected.

$$\frac{V_C(s)}{I_{load}(s)} = \frac{\frac{K_C}{s\,C}}{1 + \frac{K_C}{s\,C}\left(K_P + \frac{1}{T_i\,s}\right)\left(\frac{K_f}{1 + s\,T_{LPF}}\right)} \tag{13}$$

$$\frac{V_C(s)}{I_{load}(s)} = \frac{s(1 + s\,T_{LPF})K_C}{s^3 C T_{LPF} + s^2 C + s\,K_C K_f K_P + \frac{K_C K_f}{T_i}} \tag{14}$$

where, K_f: gain of voltage sensor, and
K_C: gain of the power converter due to energy balance between ac side and dc side.

The characteristic equation of this closed-loop transfer function must satisfy the following equation for stable operation [6].

$$(s + \alpha\zeta\omega_n)(s^2 + s\,2\zeta\omega_n + \omega_n^2) = 0 \tag{15}$$

where $\alpha > 0$, ζ (damping) > 0 and $\omega_n > 0$

If characteristic equation (14) is equated to equation (15), the value of the proportional gain, K_P and the integral time constant, T_i of the PI controller can be obtained.

$$K_P = \frac{\omega_n^2(1 + 2\zeta^2\alpha)\,C\,T_{LPF}}{K_C K_f} \tag{16}$$

$$T_i = \frac{K_C K_f}{\alpha\zeta\omega_n^3 C T_{LPF}} \tag{17}$$

The values of K_P and T_i for various α (0.01 – 75) and ζ (damping: 0.5 – 1) are shown in the Figure 10 and 11. T_{LPF} is chosen based on a filter cut-off frequency of 40Hz.

5. CASE STUDY A THREE-PHASE SHUNT ACTIVE POWER FILTER WITH MIXED LOADS

Using the stability requirement and controllability boundaries as mentioned above, the parameters for the three-phase active power filter are set up to handle a mixed load. The system in Figure 1 is tested using computer simulation to verify the concepts discussed in the previous sections. $V_{PCC\text{-}rms}$ = 1pu, V_C = 3.3333pu, L_L = 0.8%, and I_{base} = 10A

The three-phase current waveforms of the mixed loads and their *di/dt* are shown in Figure 12. The loads consist of a three-phase inductive (linear) load, single-phase diode rectifiers with RC load connected in phase A and C, and a three-phase diode rectifier with RL load. Each phase-current is compared individually to the boundaries of controllability according to (7). The phase-A load current is chosen for presentation as it has the highest rate of change. For the first case, X_{inv} = 1.96% is chosen based on a comparison between the maximum *di/dt* value of the loads in Figure 12 and the boundaries of controllability in Figure 6 (with f = 50Hz). As a result, full controllability is obtained (Figure 13) and the active power filter can compensate the reactive and harmonic currents successfully (Figure 14).

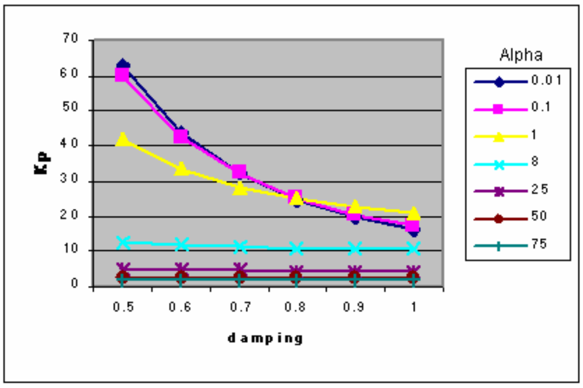

Figure 10 K_P versus damping for varying α

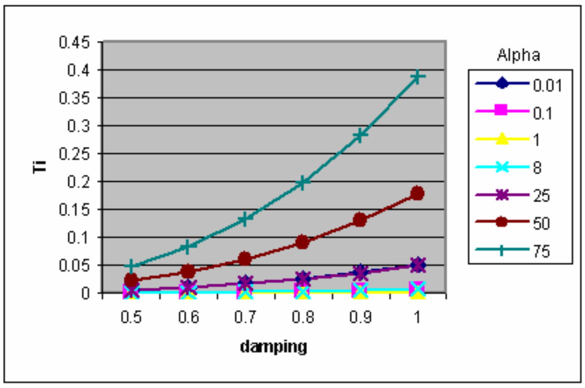

Figure 11 T_i versus damping for varying α

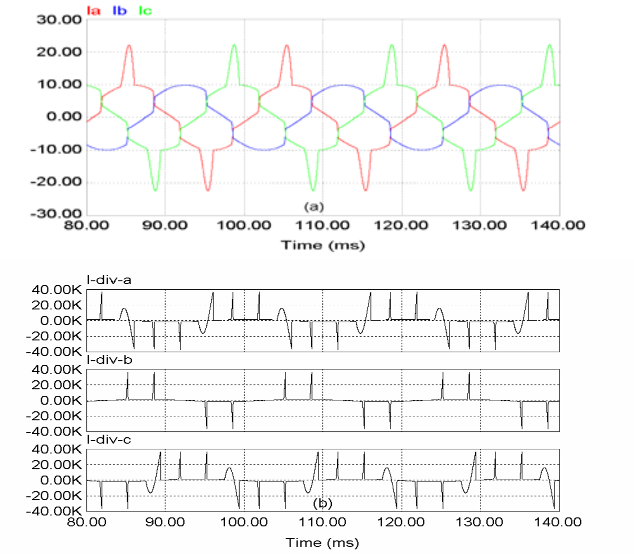

Figure 12 (a) Load currents and (b) their di/dt

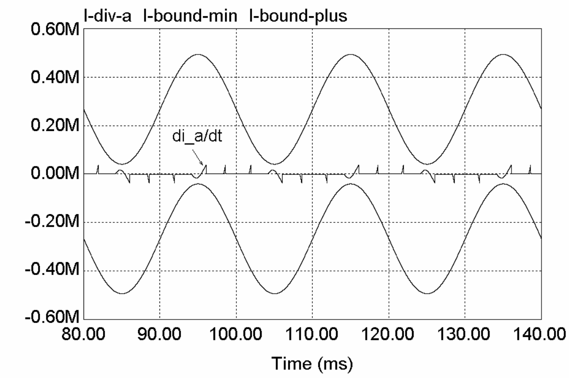

Figure 13 The di/dt of the load (phase A) is inside the boundaries

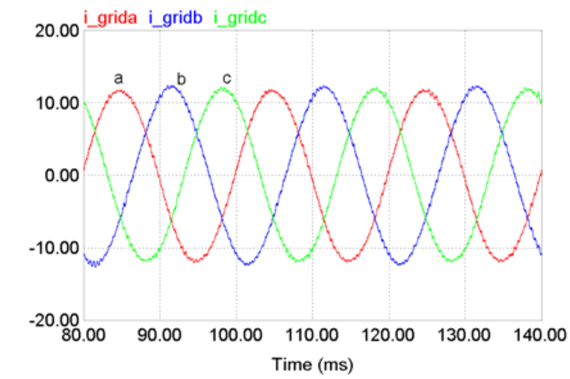

Figure 14 The grid currents after successful compensation

Alternatively, if X_{inv} is increased to 8.04%, the *di/dt* signals of the load exceed the boundary envelopes at the spot indicated (Figure 15). At that moment, the controllability of the current controller is lost since the current error signal moves away from zero. However, as soon as the *di/dt* of the loads is returned to the inside of the envelope, controllability is recovered, and the APF is able to force the grid current to return to the reference value. Overall, the active power filter fails to compensate the reactive and harmonic currents completely and the grid currents are distorted (Figure 16).

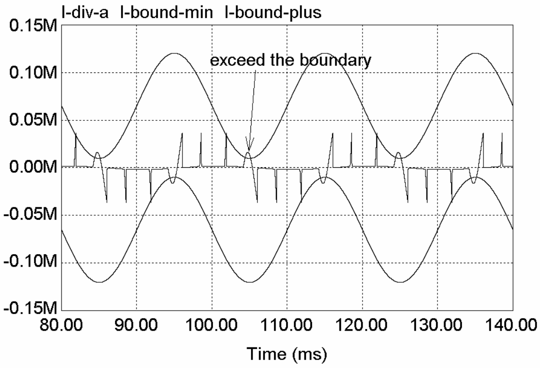

Figure 15 The di/dt of the load (phase A) exceeds the boundaries

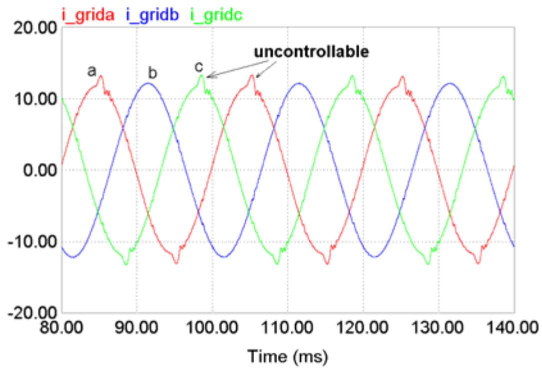

Figure 16 The grid currents due to momentary unsuccessful compensation

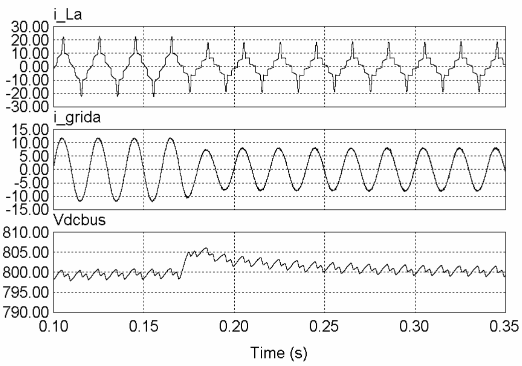

Figure 17 Dynamic condition of DC bus voltage

For the voltage control loop, according to equation (16) and (17), and Figures 10 and 11, K_p and T_i are selected for a specific α and ζ to obtain the optimum dynamic response. T_i must be chosen such that the speed response of the voltage control loop is sufficiently slower than the current control loop. Hence, both loops are decoupled. Figure 17 shows the simulation results of the dynamic condition of the dc-bus voltage for $K_P = 10$ and $T_i = 0.0058$. It can be seen that the dc-capacitor voltage is increased when the load is decreased. Once the transient interval is finished, the dc-bus voltage is recovered and remains at the reference voltage.

6. CONCLUSION

It is important to assure that APF operates successfully by checking the stability and controllability of the current control and voltage control loop of APF. The stability requirement for the current control loop is to ensure v_C is much greater than v_{PCC}. However, to maintain perfect tracking of the reference signals, the *di/dt* of the loads has to be inside of boundaries of controllability, which are established by the APF components. At the same time, the voltage control loop must be regulated so that its poles are located on the left side of the *s*-plane.

7. REFERENCES

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